



## **Ashling and Imperas Partner to Extend the RISC-V Ecosystem** *RISC-V Community Gets a Turnkey Software Solution Via Ashling / Imperas Alliance*

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**NUREMBERG, Germany -- Embedded World 2018** - [Ashling Systems](#) (a subsidiary of the NeST Group) and [Imperas Software](#) today announced a partnership to provide integrated tools and solutions for RISC-V software development. The technology aspects of this alliance include the integration of Imperas' high-performance virtual platforms, simulation engines and models into Ashling's own RiscFree™ IDE and tools offering. On the business side, Ashling will promote, sell and support this new, comprehensive, turnkey solution spanning the solutions of both companies.

As leaders in the RISC-V initiative, both companies believe that the market demands an expanded ecosystem, a turnkey solution, and one-stop shopping for RISC-V development tools. Ashling is taking the lead in promoting and selling its RiscFree™ IDE integrated solution for RISC-V software development, debug and modeling.

“We are excited about our new closer relationship with Ashling in expanding the RISC-V ecosystem and market. Imperas simulation solutions and verification models, combined with Ashling tools, offer many benefits to RISC-V customers. It is essential for RISC-V silicon developers to use commercial grade high quality simulation solutions and Ashling's worldwide sales and marketing outreach will leverage these benefits,” commented Simon Davidmann, CEO of Imperas Software.

“It's great to be partnering with the leader in processor models and virtual platforms for embedded software development,” said John Murphy, Managing Director of Ashling Microsystems Ltd (Ireland)

“Our integration with Imperas brings Ashling closer to our vision to become the provider of a complete RISC-V turnkey solution,” said Guy Rabbat, President and CEO of Ashling Systems Corporation.

“We are proud that the Ashling team focuses on the future and where technology is heading, versus just the current situation. This alliance is a strong reflection of our ambition at NeST/Ashling to always look at where the ball is going to be, not where the ball is,” said J.K. Hassan, Chairman of the NeST Group.

RISC-V is an open architecture ISA under the governance of the [RISC-V Foundation](#). It comes with many benefits such as enabling the open source community to improve and test embedded cores, ensuring trust and certifications, and portability at no additional cost.

“We are happy to see this alliance between two major members of our RISC-V Foundation. RISC-V has the potential to change the way SoCs and embedded systems are developed, and the business models around that. To achieve this potential, a solid ecosystem is needed, including RISC-V community members working together to build solutions that are greater than the sum of the individual pieces,” said Rick O’Connor, Executive Director of the non-profit RISC-V Foundation.

Ashling now delivers everything needed to develop a RISC-V application using either a real-time setup environment or pre-hardware simulation and modeling environment. Ashling debug tools will now include full IDE, RISC-V compilation, RTOS-aware debugging, JTAG probe, trace, and the full suite of simulation and hardware modeling.

Ashling’s RiscFree™ IDE for RISC-V is now available directly from Ashling. For more information, visit [www.ashling.com](http://www.ashling.com)

For more information about Imperas, please see [www.imperas.com](http://www.imperas.com).

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