Ashling announces Ashling's *RiscFree*™ C/C++ SDK support for Codasip's RISC-V-based L31 Core

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Embedded tools developer Ashling today announced support for the L31 low-power RISC-V processor core from Codasip in Ashling's ***RiscFree*** software development kit (SDK) and ***Opella-XD*** Debug Probe.

RiscFree is Ashling's SDK including an IDE, compiler and debugger and provides software development, debug & trace support for RISC-V. Since its introduction, Ashling's ***RiscFree*** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development.

Codasip L31 is a low-power, general-purpose, embedded RISC-V CPU providing an ideal balance between performance and power consumption. From IoT devices to industrial and automotive control, or as a deeply embedded core in a larger system, this versatile CPU brings local processing capabilities into a compact area.

"Strong collaboration and proven integrations are keys to unlocking the potential of RISC-V. We are glad to see Ashling's debug tools support Codasip cores. This will help our joint customers develop solutions and get to market faster with their product based on our versatile L31 core." **- Mike Eftimakis, VP Strategy and Ecosystem, Codasip.**

"*We're delighted to now include support for Codasip's L31 RISC-V processor and both our engineering teams are lined up for further collaboration ensuring upcoming L31 core debug and trace features are supported as they become available as well as support for other members of the Codasip RISC-V family.*"**- Hugh O'Keeffe, CEO of Ashling**.
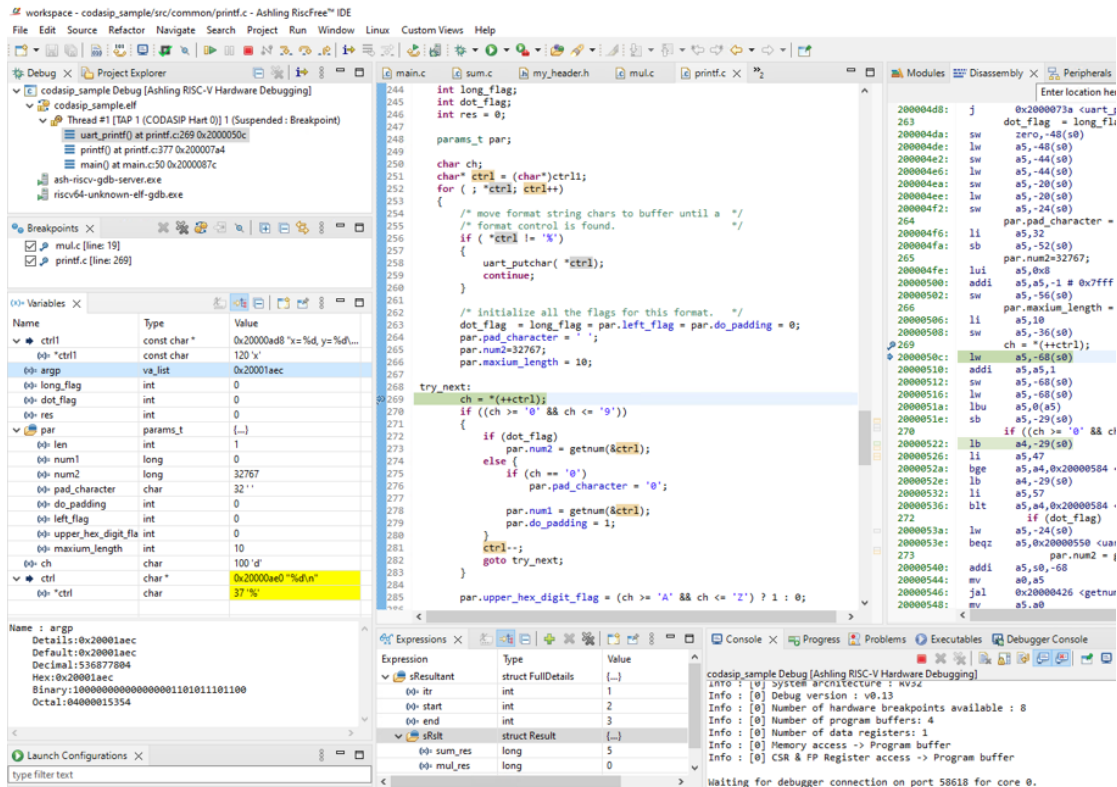
Ashling's RiscFree SDK Debug View

Ashling **RiscFree** SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multi-core debug support
- **RiscFree** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box"
- Automatic source-code formatting, syntax colouring & function folding
- Integrated compiler toolchain
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators
- High-level RISC-V register viewer
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples

For more information on Ashling's **RiscFree** see: https://www.ashling.com/ashling-riscv/ and for details on Codasip's L31 RISC-V core: https://codasip.com/products/low-power-embedded-risc-v-processors/

About Ashling

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit www.ashling.com for more details.

About Codasip

Codasip is a leading RISC-V processor technology company. Visit https://codasip.com/ for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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