ASHLING

Experts in Embedded Development Tools & Services

www.ashling.com

Ashling April 2024 News

Ashling will be attending the Embedded World Conference in Nuremberg (April-9 to 11) followed by the European RISC-V Summit in Munich (June-24 to 28) where we'll be showcasing our latest embedded development tools & solutions, including:

- Ashling's ***RiscFree™ SDK***: A complete development environment for RISC-V which now includes our new ***RiscFree*** Visual Studio Code Extension, offering full RISC-V development support within the Microsoft Visual Studio Code environment.
- ***Vitra-XS*** Debug and Trace Probe: Designed for embedded development, this probe supports multiple target architectures, including RISC-V systems with N-Trace and E-Trace, and Arm systems using CoreSight™ trace technologies (ETM, PTM, etc.). It integrates seamlessly with Ashling's recently enhanced ***RiscFree™*** debugger, now featuring new Profiling, Code-coverage, and Dynamic Function-flow Timeline views.

- ***Opella-XD*** and ***Opella-LD*** Debug Probes: Ideal for both single and multi-core, heterogeneous and homogeneous designs.
- ***TraceLLM*** our AI-driven, analysis engine designed by Ashling to enhance RISC-V based systems debug and trace exploration. Built to work seamlessly within Ashling's RiscFree Debugger, TraceLLM offers unprecedented insights into your program's real-time behaviour through an intelligent trace capture and analysis engine which can be queried using a natural language, prompt-based interface.

Some other highlights so far from 2024 include ***RiscFree*** C/C++ SDK support for:

- More and more RISC-V powered devices including the newly launched Synopsys ARC-V, Codasip's RISC-V-based L31 Core and MIPS RISC-V ISA compatible P8700 and I8500 CPUs.
- Of course, we are continuing to keep up to date with Altera's (an Intel company) FPGA roadmap and now have support for the latest Agilex™ 5 FPGA Family including debug support for the dual-core A55 and dual-core A76 Arm processors. More on this very soon.
- We have added ***RiscFree*** source-level debug support for the Rust system-level programming language with its focus on safety and concurrency without sacrificing performance and are currently working on the integration of CHERI technology (particularly for RISC-V) which further enhances system security through hardware-level (ISA) based protections.

Finally, are you struggling to make generic off-the-shelf SDKs work for your SoC? Let us create a custom solution tailored and optimized for your device's unique features – whether that's custom instruction extensions, specific pipelining or caching arrangements, hardware accelerators, CHERI support, or handling multiple heterogeneous or homogeneous cores. Contact us for a complimentary consultation with our tool experts (email: sales@ashling.com) and discover how our custom solutions, including Debuggers, IDEs, Compiler Toolchains, Simulators, Debug & Trace Probes, Reference Boards, OS/RTOS ports, and more, can perfectly fit your needs.

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Cochin India and sales and support offices in Europe, Asia Pacific, the Middle East and America. Visit www.ashling.com for more details.

Contacts

Email info@ashling.com or see https://www.ashling.com/contact-ashling/

All trademarks, logos and brand names are the property of their respective owners.