Ashling announces *RiscFree*™ C/C++ SDK support for Lattice RISC-V MCU CPU Soft IP Cores

Limerick, Ireland – July 14, 2023 – Ashling today announced its ***RiscFree*** SDK has been added to the Lattice Semiconductor RISC-V® MC CPU soft IP support ecosystem.

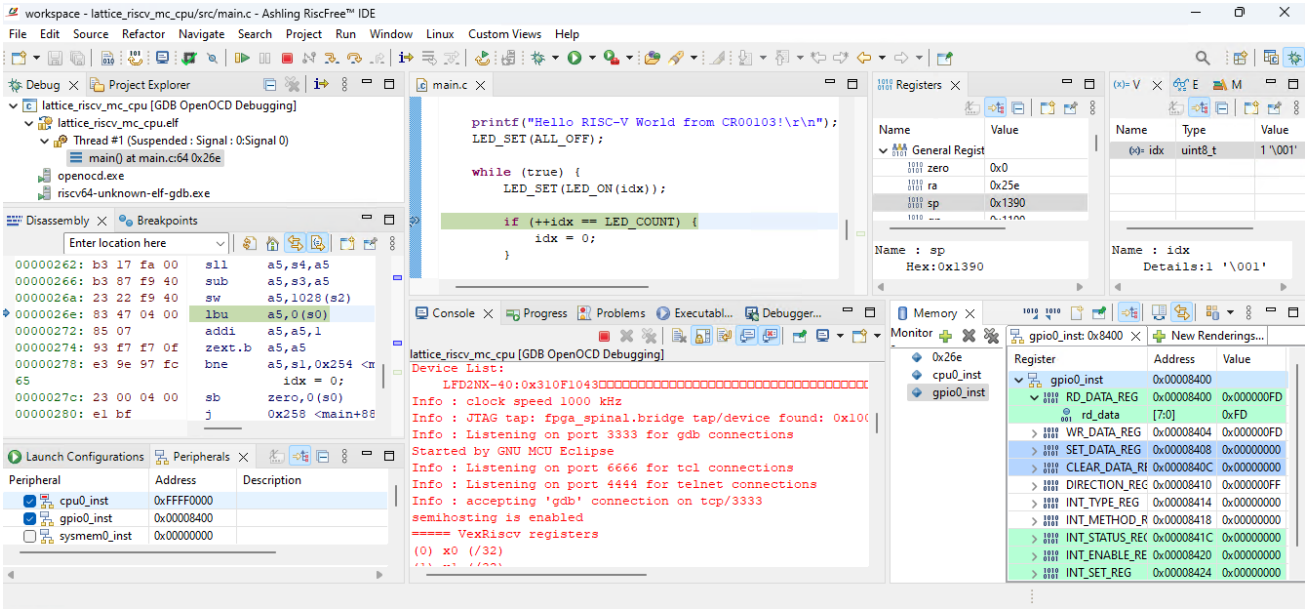
RiscFree is Ashling's SDK including an IDE, compiler and debugger, which now provides software development and debug support for Lattice's RISC-V MCU CPU soft IP. Since its introduction, Ashling's ***RiscFree*** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development.

"We are pleased to announce support for Lattice's RISC-V MCU CPU soft IP cores and that our RiscFree is now part of Lattice's tools eco-system for development and debugging. We're looking forward to enhanced collaboration, particularly between our engineering teams, to ensure that RiscFree is positioned to exploit all additional debugging and analysis capabilities planned for future MCU CPU IP devices" said **Hugh O'Keeffe, CEO of Ashling**.

"*Enabling our customers to innovate without constraints is a top priority at Lattice. We are excited to welcome Ashling to our growing partner ecosystem and to open up even more ways for our customers to achieve their design goals with our power efficient FPGAs*" said **Karl Wachswender, Principal System Architect at Lattice Semiconductor.**

Ashling ***RiscFree*** SDK support for Lattice's MCU CPU soft IP includes:

- IDE with full source & project creation, editing, build & debug support
- ***RiscFree*** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box"
- Automatic source-code formatting, syntax colouring & function folding
- Integrated compiler toolchain
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators
- High-level RISC-V register viewer
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples



Ashling's RiscFree SDK Debug View

For more information on Ashling's ***RiscFree*** see: https://www.ashling.com/ashling-riscv/ and for details on Lattice's MCU CPU soft IP see: https://www.latticesemi.com/products/designsoftwareandip/intellectualproperty/ipcore/ipcores04/riscvmccpu

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East and America. Visit www.ashling.com for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of the RISC-V International. Visit https://riscv.org for more details.

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