Ashling's RiscFree™ SDK Toolchain now available with support for MIPS RISC-V ISA compatible P8700 and I8500 CPUs

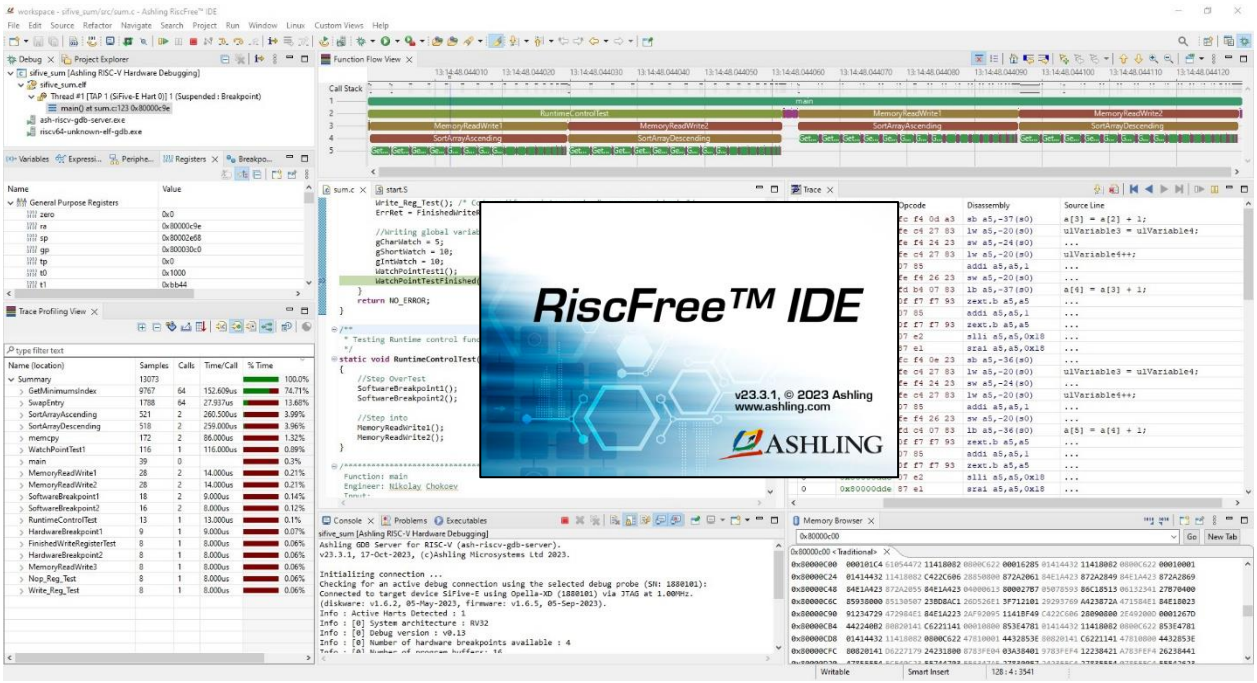
Feb 23, 2023

SILICON VALLEY, CA, USA. Ashling and MIPS announced today that Ashling's ***RiscFree*** SDK is now available with full support for MIPS RISC-V ISA based CPUs including the P8700 and I8500. ***RiscFree*** is Ashling's Integrated Development Environment (IDE) including a compiler and debugger for RISC-V based development, and it now has support for MIPS RISC-V ISA based CPUs, enhanced by MIPS' own proven and tested Core Framework Platform.

*"We are delighted to have working Ashling **RiscFree** support for our RISC-V ISA IP cores. Our engineering teams have worked closely together developing the toolchain in parallel with the core IP and believe this will result in rapid time-to-market for our end customers,"* said **Rick Leatherman, Senior Director at MIPS**.

The Ashling ***RiscFree*** toolchain includes support for both code development and debug on MIPS CPUs and includes advanced features such as multi-core and multi-cluster support, Linux debug awareness, real-time trace support, and cache awareness. It also comes with a range of Ashling hardware probes supporting debug and trace. In addition, a targeted and optimised GCC toolchain is included and fully integrated into the ***RiscFree*** IDE.

*"We are excited to see MIPS, one of the first companies to bring a RISC based architecture to the market back in the 1980s, now expanding to offer RISC-V ISA compliant cores. We've a long history of working together and believe the support of our market-leading **RiscFree** Toolchain will help in the rapid market adoption of their MIPS RISC-V ISA cores,"* said **Hugh O'Keeffe, CEO of Ashling**.



Ashling's RiscFree SDK Debug & Trace View

In addition to ***RiscFree***, the Ashling hardware probes including the ***Opella-XD*** JTAG debug probe and the ***Vitra-XS*** debug & trace probe also provide full support for MIPS P8700 and I8500 CPUs.

About Ashling
Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit www.ashling.com for more details.

About MIPS
MIPS is accelerating compute density in the automotive, cloud and embedded markets. Giving customers the freedom to build unique products for specific workloads, MIPS' industry-leading cores are configurable, efficient and easy to implement. Its multi-threading methodology delivers advanced scalability and the ability to efficiently move and process data faster. The company's compute DNA spans more than two decades with billions of MIPS-based chips shipped to date. For more information, visit www.MIPS.com.

About RISC-V
The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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