

Ashling RiscFree™ now supports Alibaba's RISC-V CPUs

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SAN FRANCISCO, CA USA - RISC-V Summit 2021 – Ashling announced today that Ashling's **RiscFree™** Toolchain will be extended to support the broad range of Alibaba RISC-V CPU IPs including support for the open source XuanTie E902, E906, C906, and C910.

RiscFree™ is Ashling's Integrated Development Environment (IDE), Compiler and Debugger for RISC-V based development and now adds support for Alibaba RISC-V CPUs including the 32-bit and the 64-bit cores.

"We're happy to add support for Alibaba as one of the leading RISC-V core vendors. Ashling's **RiscFree™** with its *Different Cores, One Solution* feature set now brings the power of heterogeneous, multi-core debugging to Alibaba's RISC-V CPU users allowing a single instance of **RiscFree™** to debug any number of heterogeneous and homogeneous cores" said Hugh O'Keeffe, Managing Director of Ashling.



Alibaba T-Head's open source RISC-V-based Xuantie series processors

For more information on Ashling's **RiscFree™** see: <https://www.ashling.com/ashling-riscv/>

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Chennai India and sales and support offices in Europe, Asia Pacific, the Middle East and America. We have over thirty years' experience in developing tools for embedded systems engineers including high-speed Debug and Trace Probes supporting a broad range of MCUs, SoCs and Soft (FPGA) based designs. Our software tools include IDEs, Debuggers, Compilers and Simulators and we support all the main embedded architectures including ARC, Arm, MIPS, Power Architecture and RISC-V through our RiscFree™ platform. We have a particular focus on RISC-V and are the first company to bring tools to the market supporting heterogeneous debug of RISC-V cores along with cores from other vendors. Visit www.ashling.com for more details or contact Nadim Shehayed: nadim@ashling.com

About RISC-V

RISC-V open architecture ISA is under the governance of the RISC-V Foundation. Visit <https://riscv.org> for more details

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