



Ashling announce **RiscFree™ C/C++ SDK** support for the newly launched Synopsys ARC-V RISC-V ISA based Processors

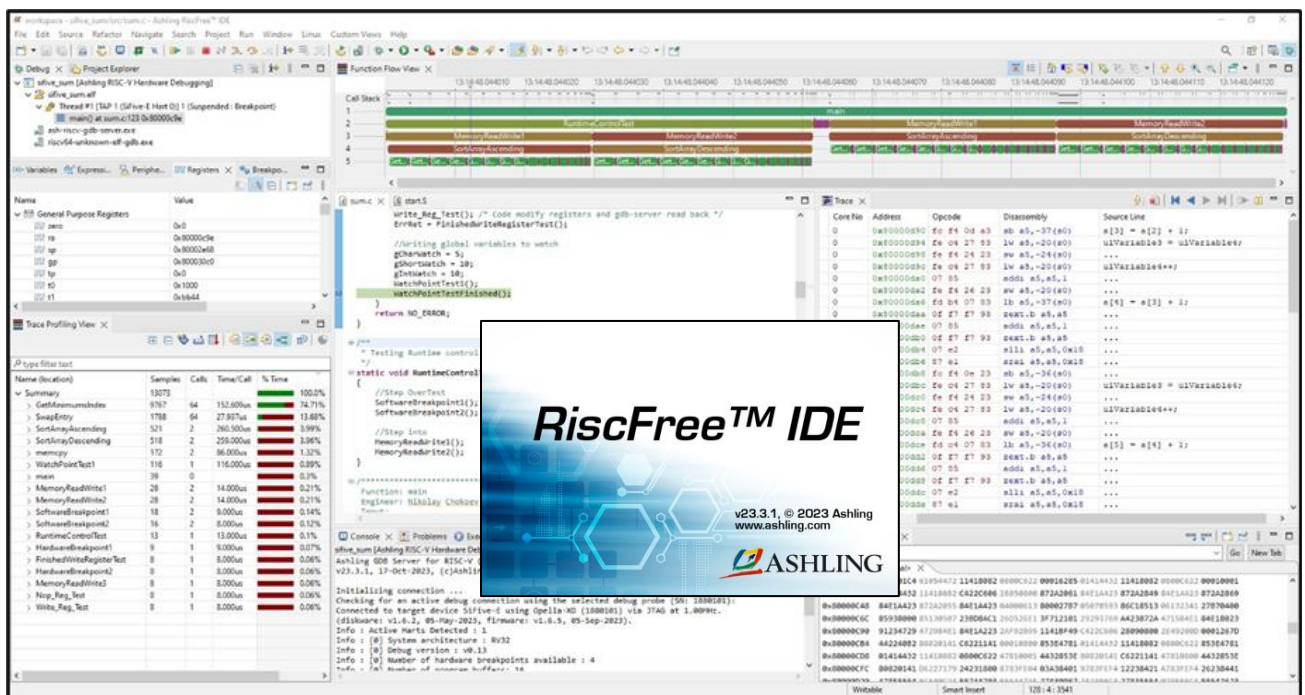
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Ashling today announced support for the Synopsys ARC-V RISC-V ISA compliant Processor family.

“Ashling, as a long-term Synopsys partner for over fifteen years and a provider of Debug and Trace probe solutions for Synopsys ARC® Processor users, is excited about the launch of the new Synopsys ARC-V™ Processor IP based on the RISC-V ISA. The news that Synopsys, as one of the world’s leading providers of Processor IP, is adopting the RISC-V ISA reiterates the sheer momentum behind RISC-V and it’s mounting influence in our industry.

As one of the leading members of the RISC-V tools ecosystem, we’re very excited to continue working closely with Synopsys, ensuring that our RiscFree™ SDK, synonymous with RISC-V, supports the new Synopsys ARC-V Processor family.” - Hugh O’Keeffe, CEO of Ashling.

RiscFree is Ashling’s SDK including an IDE, compiler and debugger and provides software development and hardware debug & trace support for RISC-V. Since its introduction, Ashling’s **RiscFree** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support has made it the go-to choice for 32-bit and 64-bit RISC core software development.



Ashling’s RiscFree SDK Debug View

In addition to **RiscFree**, the Ashling hardware probes including the **Opella-XD** debug probe and **Vitra-XS** debug & trace probe also provide full support for ARC-V offering a convenient migration path for existing ARC Processor users of these tools.

About Ashling:

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit www.ashling.com for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit <https://riscv.org> for more details.

Ashling Contact

Contact info@ashling.com or visit <https://www.ashling.com/contact-ashling/>

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