



Ashling RiscFree™ now supports Andes Technology RISC-V CPUs

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SAN FRANCISCO, CA USA - RISC-V Summit 2021. Ashling and Andes Technology announced today that Ashling's **RiscFree™** Toolchain will be extended to support the broad range of Andes RISC-V CPU IPs including support for the AndeStar™ V5 Performance and CoDense™ ISA Extension, leveraging the high-quality and production-proven Andes GNU compiler.

RiscFree™ is Ashling's Integrated Development Environment (IDE), Compiler and Debugger for RISC-V based development and now adds support for Andes RISC-V CPUs including the 32-bit: N22, N25F, D25F, A25, A25MP, A27, A27L2, N45, D45, A45 & A45MP and the 64-bit: NX25F, AX25, AX25MP, NX27V, AX27, AX27L2, NX45, AX45 & AX45MP.

"Ashling's **RiscFree™** with its *Different Cores, One Solution* feature set now brings the power of heterogeneous, multi-core debugging to Andes RISC-V CPU users allowing a single instance of **RiscFree™** to debug any number of heterogeneous and homogeneous cores" said Hugh O'Keeffe, Managing Director of Ashling.

"We are delighted to have Ashling **RiscFree™** support Andes RISC-V CPU cores and offer an additional choice for our customers, particularly those working on heterogeneous SoC designs utilizing AndeCore™ V5 RISC-V processors with increased performance and reduced code size" said Dr. Charlie Su, Andes Technology President and CTO.

For more information on Ashling's **RiscFree™** see: <https://www.ashling.com/ashling-riscv/> and for details on Andes RISC-V CPU cores see: <http://www.andestech.com/en/products-solutions/andescore-processors/>.

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Chennai India and sales and support offices in Europe, Asia Pacific, the Middle East and America. We have over thirty years' experience in developing tools for embedded systems engineers including high-speed Debug and Trace Probes supporting a broad range of MCUs, SoCs and Soft (FPGA) based designs. Our software tools include IDEs, Debuggers, Compilers and Simulators and we support all the main embedded architectures including ARC, Arm, MIPS, Power Architecture and RISC-V through our **RiscFree™** platform. We have a particular focus on RISC-V and are the first company to bring tools to the market supporting heterogeneous debug of RISC-V cores along with cores from other vendors. Visit www.ashling.com for more details.

Contact Nadim Shehayed: nadim@ashling.com

About Andes Technology

Sixteen years in business and a Founding Premier member of RISC-V International, Andes is a leading supplier of high-performance/low-power 32/64-bit embedded processor IP solutions, and a main force to take RISC-V mainstream. Andes' fifth-generation AndeStar™ architecture adopted the RISC-V as the base. Its V5 RISC-V CPU families range from tiny 32-bit cores to advanced 64-bit cores with DSP, FPU, Vector, Linux, superscalar, and/or multicore capabilities. The annual volume of Andes-Embedded SoCs has exceeded 2 billion since 2020 and continues to rise. To the end of 2020, the cumulative volume of Andes-Embedded™ SoCs has reached 7 billion. For more

information, please visit <https://www.andestech.com>. Follow Andes on [LinkedIn](#), [Twitter](#), [Facebook](#), and [YouTube](#)!

Contact Hsiao-Ling Lin: hllin@andestech.com

About RISC-V

The RISC-V open architecture ISA is under the governance of the RISC-V International. Visit <https://riscv.org> for more details