Ashling unlocks full RiscFree™ Debug and Trace for Mirafra's "Ramanujan" RISC-V & Arm based SoC

Silicon Valley, CA – Feb-16, 2026 – Ashling today announced full debug and trace support for Mirafra's "Ramanujan" 22-nm SoC within its RiscFree SDK.

RiscFree provides comprehensive visibility and control across the entire software stack—from low-level drivers to high-level application code. With features including breakpoints, step/continue execution, register and memory inspection, real-time trace, and multi-core support (both homogeneous and heterogeneous), ***RiscFree*** enables efficient debugging, tracing and performance tuning of complex embedded systems. This collaboration ensures that developers targeting Mirafra's high-performance *"Ramanujan"* SoCs can now rely on a robust and proven tool chain to accelerate development, debugging, and system validation.

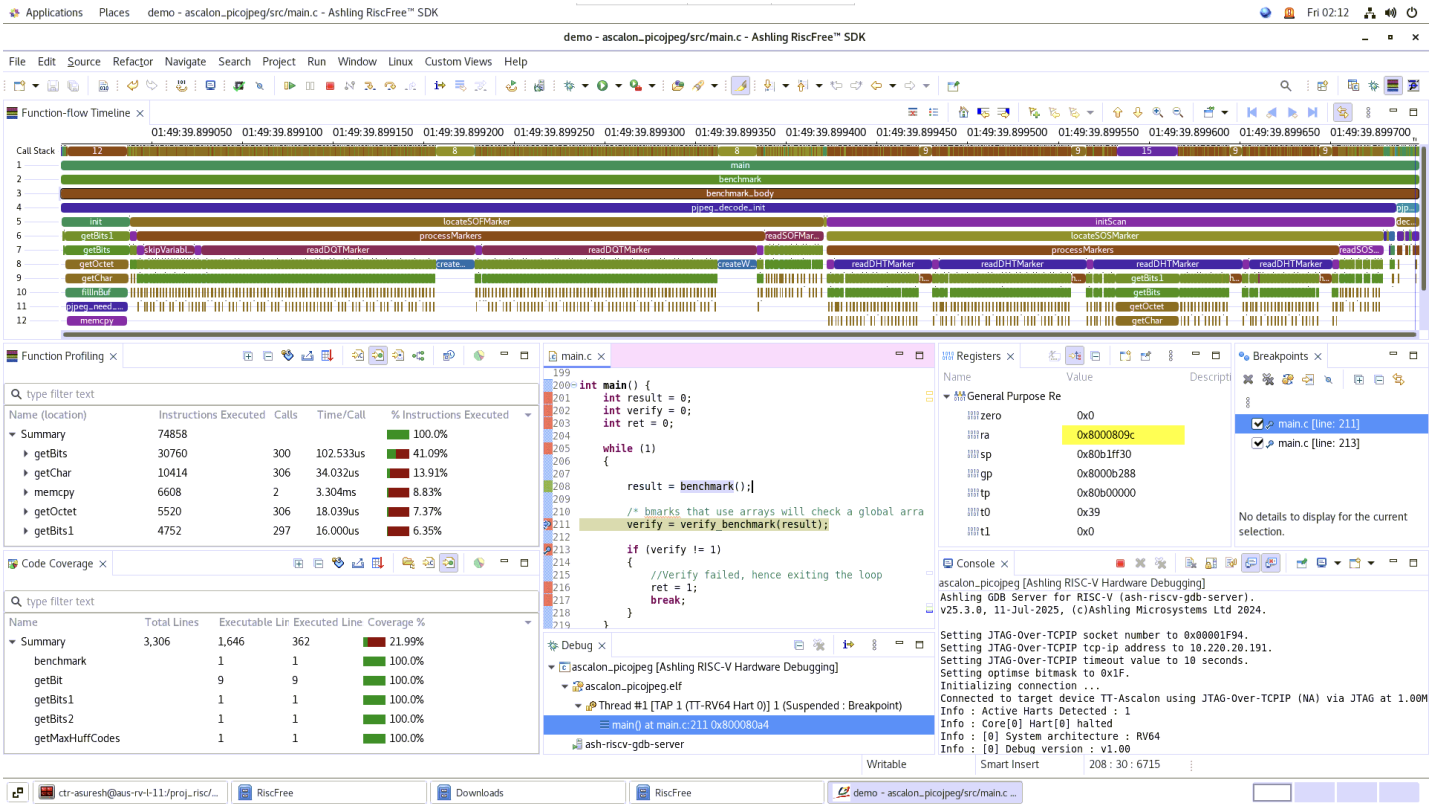

Figure 1. Ashling's *RiscFree* debugging and tracing support.

"*The Ramanujan SoC showcases Mirafra's ability to deliver complete taped-out, silicon platforms and partnering with Ashling ensures developers have a proven debug and trace environment from day one*," said ***Alok Kuchlous, CEO of Mirafra.***

"Ashling's technical expertise was pivotal in accelerating the debug subsystem bring-up for the Ramanujan project's heterogeneous dual cores (ARM A55 and Incore Azurite RISC-V)," said ***Anoop Oruvingal, Mirafra Project Manager for the Ramanujan SoC.***

"*Ramanujan*" (named after the famous Indian mathematician) is built around a dual network-on-chip (NoC) architecture that separates application processing from secure boot and system control functions, while allowing AXI-based (Advanced eXtensible Interface) communication between the two domains. The SoC integrates a single-core Arm Cortex-A55 application processor alongside a separate InCore RISC-V Azurite core for system and secure functions. The SoC supports external memory through SDRAM, Flash, and HyperRAM interfaces, along with on-chip SRAM and standard DMA-based data movement.

"Ramanujan's split between application and secure system domains is exactly where embedded software teams need clear visibility, and RiscFree is built for this kind of heterogeneous system, letting engineers debug Arm and RISC V cores in a single, unified session with simultaneous control and trace where needed, so they can move fast from first boot to stable software and validated systems," said ***Hugh O'Keeffe, CEO of Ashling****.*

About Mirafra

Mirafra is a leading technology services company with expertise in software development and silicon design services. Founded in 2004, we offer a wide range of solutions to our clients and are committed to providing them with the highest quality. We have a global presence with our headquarters in Bangalore and design and business centers in Houston, Austin, San Jose, San Diego, New Jersey, Sweden, Singapore, Pune, and Chennai. Our exceptional team of engineers collaborates with all the major tier 1 and tier 2 companies in India, the USA, Europe, and Malaysia.
Learn more at https://www.mirafra.com/

About Ashling

Ashling is a world leader in the development of tools and solutions for embedded systems and the semiconductor industry. With a focus on enabling software design for next-generation processors and SoCs, Ashling offers cutting-edge debugging tools, trace probes, and development environments. Learn more at https://www.ashling.com/