Ashling announces *RiscFree*™ C/C++ SDK support for Microchip Technologies' PIC64GX RISC-V®-based multicore MPUs

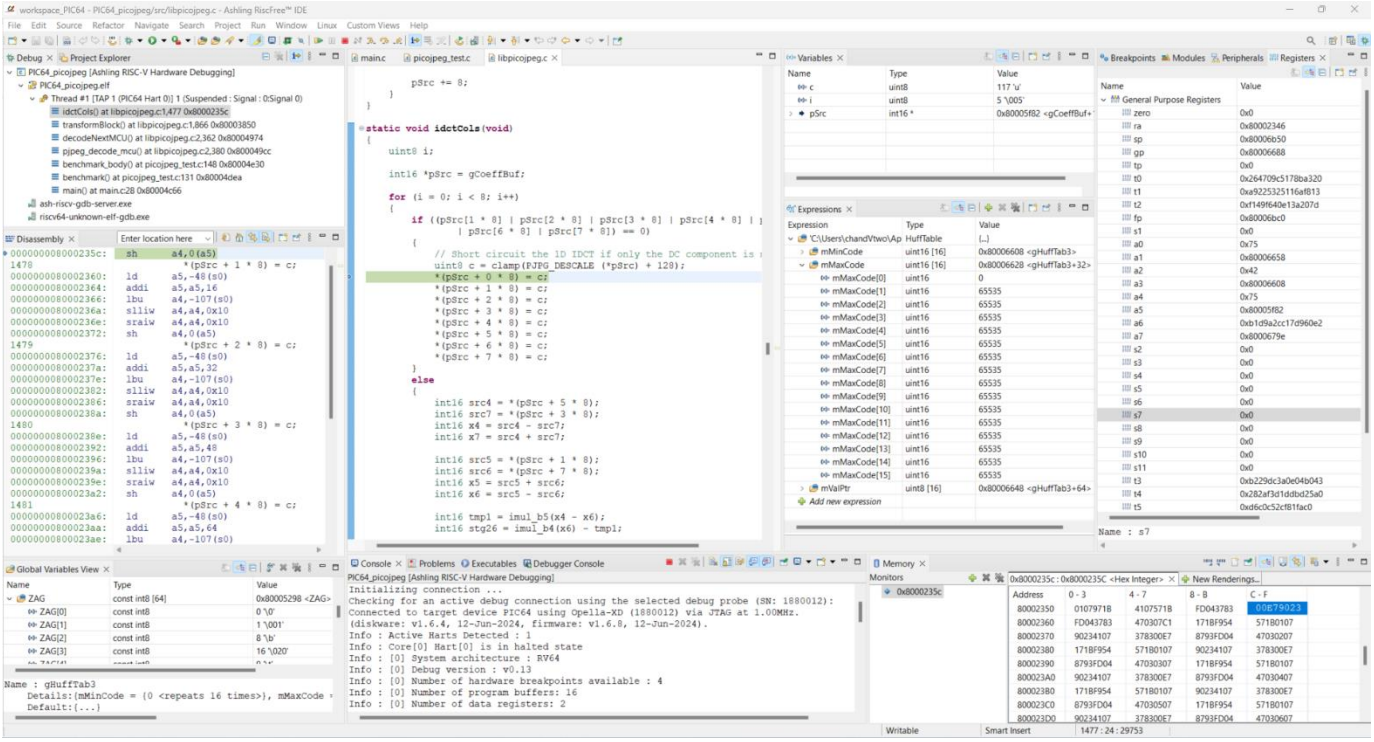
July-23rd, 2024, Limerick, Ireland. Embedded tools developer Ashling is pleased to partner with Microchip Technology, supporting the new and innovative **PIC64GX** RISC-V based multicore MPUs with our ***RiscFree*™** C/C++ SDK and ***Opella-XD*** Debug Probe.

"A wide range of tools and support systems are essential for the commercial success and accelerated development of RISC-V technologies," said ***Shakeel Peera, vice president of marketing and strategy*** *for Microchip's FPGA business unit. "Microchip's Mi-V ecosystem partner Ashling, a pioneer in RISC-V tools, allows us to offer customers a comprehensive toolchain and robust support services for our PIC64GX MPUs."*

RiscFree is Ashling's SDK including an IDE, compiler and debugger and provides software development, debug & trace support for RISC-V cores. Since its introduction, Ashling's ***RiscFree*** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development.

"*Since its introduction, Ashling's* ***RiscFree*** *SDK has been making significant strides in the embedded tools market, particularly within the RISC-V sector, due to its ease-of-use, extensive functionality, plug-in architecture, and robust multicore and real-time trace support. This collaboration with Microchip Technology not only enhances our product offerings but also capitalizes on the groundbreaking capabilities of Microchip's PIC64GX multicore RISC-V based MPU, setting a new standard for 64-bit RISC-V software development tools in the microprocessor market.*" **- Hugh O'Keeffe, CEO of Ashling**.

RiscFree C/C++ SDK



Ashling's RiscFree SDK Debug View

Ashling ***RiscFree*** SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multicore debug support.
- ***RiscFree*** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Automatic source-code formatting, syntax colouring & function folding.
- Integrated compiler toolchain.
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators.
- High-level RISC-V register viewer.
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples.

For more information or to download a free evaluation of Ashling's ***RiscFree*** see: https://www.ashling.com/ashling-riscv/ and for details on Microchip Technologies' PIC64GX RISC-V MPUs visit here: https://www.microchip.com/en-us/products/microprocessors/64-bit-mpus/pic64gx

About Ashling

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company is well known for its ***RiscFree*** SDK supporting Arm-Cortex and RISC-V and is the first to bring to the market in a single toolchain support for heterogeneous, multicore development and debugging of any combination of RISC-V cores with Arm-Cortex cores. Visit https://www.ashling.com/ for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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