Ashling announces *RiscFree*™ C/C++ SDK support for Renesas's RISC-V-based R9AG021 MCUs

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Embedded tools developer Ashling today announced support for the Renesas R9AG021 RISC-V MCUs from Renesas in Ashling's ***RiscFree*** software development kit (SDK) and ***Opella-XD*** Debug Probe.

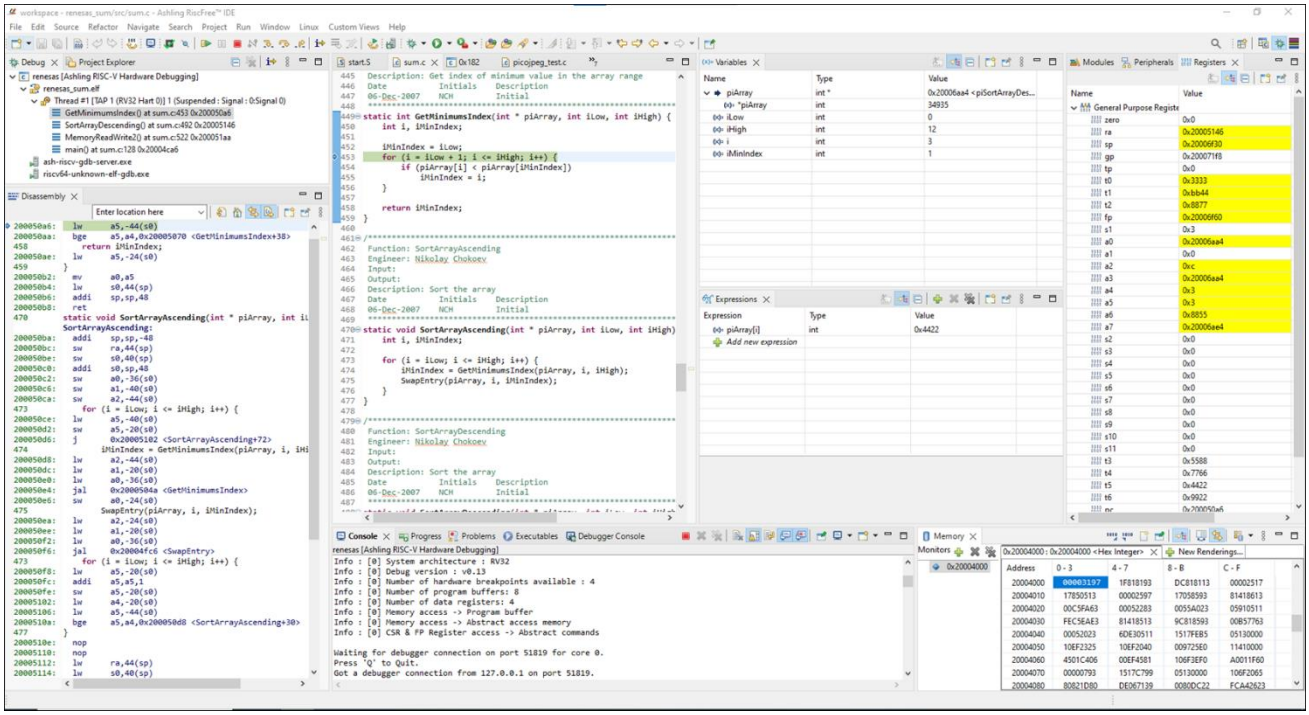
RiscFree is Ashling's SDK including an IDE, compiler and debugger and provides software development, debug & trace support for RISC-V. Since its introduction, Ashling's ***RiscFree*** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development.

As the world leader in MCUs, **Renesas** ships more than 3.5 billion units per year, with approximately 50% of shipments serving the automotive industry, and the remainder supporting industrial and Internet of Things applications as well as data centre and communications infrastructure. The new Renesas R9AG021 group of MCUs is the first, Renesas developed RISC-V based general-purpose MCU providing an ideal balance between performance and power consumption.

"Broad tools and ecosystem choices are fundamental in ensuring RISC-V commercial success and quick time to market. We are pleased to have a leading supplier like Ashling strengthen the offering to our customers and provide strong support for our RISC-V general-purpose MCUs with a complete toolchain." **- Daryl Khoo, Vice President of Embedded Processing 1st Business Division at Renesas, Renesas.**

"*We're delighted to now include **RiscFree** support for Renesas' first in-house developed RISC-V MCU and both our engineering teams are lined up for further collaboration ensuring future enhancements of debug and trace features are supported as they become available as well as support for other derivatives of the Renesas R9AG021 general purpose RISC-V group.*"**- Hugh O'Keeffe, CEO of Ashling**.

RiscFree C/C++ SDK



Ashling's RiscFree SDK Debug View

Ashling ***RiscFree*** SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multi-core debug support.
- ***RiscFree*** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Automatic source-code formatting, syntax colouring & function folding.
- Integrated compiler toolchain.
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators.
- High-level RISC-V register viewer.
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples.

For more information on Ashling's ***RiscFree*** see: https://www.ashling.com/ashling-riscv/ and for details on Renesas's RISC-V MCUs visit here: https://www.renesas.com/us/en/about/press-room/renesas-unveils-first-generation-own-32-bit-risc-v-cpu-core-ahead-competition

About Ashling

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit https://www.ashling.com/ for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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