

Ashling announces *RiscFree*[™] C/C++ SDK support for

Renesas's RISC-V-based R9AG021 MCUs

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Embedded tools developer Ashling today announced support for the Renesas R9AG021 RISC-V MCUs from Renesas in Ashling's *RiscFree* software development kit (SDK) and *Opella-XD* Debug Probe.

RiscFree is Ashling's SDK including an IDE, compiler and debugger and provides software development, debug & trace support for RISC-V. Since its introduction, Ashling's **RiscFree** SDK has been steadily building market share within the embedded tools market and is particularly strong in the RISC-V market where its ease-of-use, broad functionality, plug-in architecture and real-time trace support have made it the go-to-choice for 32-bit and 64-bit RISC core software development.

As the world leader in MCUs, **Renesas** ships more than 3.5 billion units per year, with approximately 50% of shipments serving the automotive industry, and the remainder supporting industrial and Internet of Things applications as well as data centre and communications infrastructure. The new Renesas R9AG021 group of MCUs is the first, Renesas developed RISC-V based general-purpose MCU providing an ideal balance between performance and power consumption.

"Broad tools and ecosystem choices are fundamental in ensuring RISC-V commercial success and quick time to market. We are pleased to have a leading supplier like Ashling strengthen the offering to our customers and provide strong support for our RISC-V general-purpose MCUs with a complete toolchain." - Daryl Khoo, Vice President of Embedded Processing 1st Business Division at Renesas, Renesas.

"We're delighted to now include **RiscFree** support for Renesas' first in-house developed RISC-V MCU and both our engineering teams are lined up for further collaboration ensuring future enhancements of debug and trace features are supported as they become available as well as support for other derivatives of the Renesas R9AG021 general purpose RISC-V group."- Hugh O'Keeffe, CEO of Ashling.

RiscFree C/C++ SDK

# workspace - renesas_sum/src/sum.c - Ashling RiscFree™ IDE						- 0 ×
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✓	445 Description: Get index of minimum value in the array range	Name	Туре	Value		8 8 8 8 8 8
✓ Prenesas_sum.elf	446 Date Initials Description	v + piArray	int *	0x20006aa4 < piSortArrayDes	Name	Value
✓ n Thread #1 [TAP 1 (RV32 Hart 0)] 1 (Suspended : Signal : 0:Signal 0)	447 06-Dec-2007 NCH Initial	(a) *piArray	int	34935	✓ M General Purpose Regis	
GetMinimumsIndex() at sum.c:453 0x200050a6	4498 static int GetMinimumsIndex(int * piArray, int iLow, int iHigh) {	(d) iLow	int	0		
SortArrayDescending() at sum.c:492 0x20005146	450 int i, iMinIndex;	60- iHigh	int	12	IIII zero	0x0
MemoryReadWrite2() at sum.c:522 0x200051aa	451	60-i	int	3	IIII ra	0x20005146
main() at sum.c:128 0x20004ca6	452 iMinIndex = iLow;	60+ iMinIndex	int	1	IIII sp	0x20006f30
ash-riscv-gdb-server.exe	<pre>9 453 for (i = iLow + 1; i <= iHigh; i++) { if (piArray[i] < piArray[iMinIndex])</pre>	NO. INNIHITARY	an.		IIII gp	0x200071f8
riscv64-unknown-elf-gdb.exe	454 if (piArray[i] < piArray[iMinIndex]) 455 iMinIndex = i;				IIII tp	0x0
	456				1111 tO	0x3333
🖭 Disassembly 🗙 💭 🗖	457				2227 11	0xbb44
Enter location here 🗸 🚷 🖄 😪 📑 😁 🖇	458 return iMinIndex;				1111 12	0x8877
© 200050a6: 1w a5,-44(s0)	459 }				IIII fp	0x20006f60
200050aa: bge a5,a4,0x20005070 <getminimumsindex+38></getminimumsindex+38>	460 4610 /****				1111 s1	0x3
458 return iMinIndex;	40107 462 Function: SortArrayAscending				1111 aO	0x20006aa4
200050ae: lw a5,-24(s0)	463 Engineer: Nikolay Chokoey				1111 a1	0x0
459 }	464 Input:				1111 a2	Oxc
200050b2: mv a0,a5 200050b4: lw s0.44(sp)	465 Output:				1111 a3	0x20006aa4
200050b4: lw s0,44(sp) 200050b6: addi sp,sp,48	466 Description: Sort the array	60 F	P			Ox3
200050b8: ret	467 Date Initials Description 468 06-Dec-2007 NCH Initial	☆ Expressions ×	S	FIEL & 24 44 1 C2 C2 8 .	1101 07	Ox3
470 static void SortArrayAscending(int * piArray, int il	469	Expression	Type	Value	2207 a6	0x8855
SortArrayAscending:	4700 static void SortArrayAscending(int * piArray, int iLow, int iHigh)	(+) piArray[i]	int	0x4422	1111 a7	0x20006ae4
200050ba: addi sp,sp,-48	471 int i, iMinIndex;	Add new expression			1111 s2	0x0
200050bc: sw ra,44(sp) 200050bc: sw s0.40(sp)	472				2007 s3	0x0
200050be: sw s0,40(sp) 200050c0: addi s0,sp,48	473 for (i = iLow; i <= iHigh; i++) (1111 54	0x0
200050c2: sw a0,-36(s0)	474 iNinIndex = GetMinimumsIndex(piArray, i, iHigh); 475 SwapEntry(piArray, i, iMinIndex);				### s5	0x0
200050c6: sw a1,-40(s0)	476 }				1111 s6	0x0
200050ca: sw a2,-44(s0)	477 }				2211 s7	0x0
473 for (i = iLow; i <= iHigh; i++) {	478				1111 58	0x0
200050ce: lw a5,-40(s0)	4798 /*****				1111 59	0x0
200050d2: sw a5,-20(s0) 200050d6: j 0x20005102 <sortarrayascending+72></sortarrayascending+72>	480 Function: SortArrayDescending				1111 s10	0x0
474 iNinIndex = GetMinimumsIndex(piArray, i, iHi	481 Engineer: Nikolay Chokoey 482 Input:				2227 s11	0x0
200050d8: 1w a2,-44(s0)	483 Output:				1111 13	0x5588
200050dc: 1w a1,-20(s0)	484 Description: Sort the array				1111 14	0x7766
200050e0: 1w a0,-36(s0)	485 Date Initials Description				1111 15	0x4422
200050e4: jal 0x2000504a <getminimumsindex> 200050e6: sw a0,-24(s0)</getminimumsindex>	486 06-Dec-2007 NCH Initial				1111 t6	0x9922
200050e6: sw a0,-24(s0) 475 SwapEntry(piArray, i, iMinIndex);	487				1111 pc	0x200050x6
200050ea: lw a2,-24(s0)	< > >				<	>
200050ee: lw a1,-20(s0)	Console X 🖏 Progress 🕐 Problems 👔 Executables 🚱 Debugger Console	**				
200050f2: 1w a0,-36(s0)		149 36 108 (MD) 104 [OH [O				
200050f6: jal 0x20004fc6 <swapentry> 473 for (i = iLow: i <= iHigh: i++) {</swapentry>	renesas [Ashling RISC-V Hardware Debugging]			Monitors 👙 💥 🗞 0x200040	100 : 0x20004000 <hex integer=""> 🗙 🍦</hex>	New Renderings
473 for (i = iLow; i <= iHigh; i++) { 200050f8: lw a5,-20(s0)	Info : [0] System architecture : RV32 Info : [0] Debug version : v0.13			Ox20004000 Address	0-3 4-7 8	-B C-F ^
200050fc: addi a5,a5,1	Info : [0] Number of hardware breakpoints available : 4			20004	00 00003197 1F818193	DC818113 00002517
200050fe: sw a5,-20(s0)	Info : [0] Number of program buffers: 8			20004		17058593 81418613
20005102: lw a4,-20(s0)	Info : [0] Number of data registers: 4			20004		0055A023 05910511
20005106: lw a5,-44(s0)	Info : [0] Memory access -> Program buffer					
2000510a: bge a5,a4,0x200050d8 <sortarrayascending+30> 477 }</sortarrayascending+30>	Info : [0] Memory access -> Abstract access memory			20004		9C818593 00B57763
477 } 2000510e: nop	Info : [0] CSR & FP Register access -> Abstract commands			20004		1517FEB5 05130000
2000510: nop	Waiting for debugger connection on port 51819 for core 0.			20004		009725E0 11410000
20005112: lw ra,44(sp)	Press 'Q' to Quit.			20004		106F3EF0 A0011F60
20005114: lw s0,40(sp) *	Got a debugger connection from 127.0.0.1 on port 51819.			v 20004	070 00000793 1517C799	05130000 106F2065
(C		>	20004	080 80821D80 DE067139	0080DC22 FCA42623 *

Ashling's RiscFree SDK Debug View

Ashling RiscFree SDK support for includes:

- IDE with full source & project creation, editing, build & integrated multi-core debug support.
- **RiscFree** includes a single-shot installer that installs & automatically configures all the component tools to work "out-of-the-box".
- Automatic source-code formatting, syntax colouring & function folding.
- Integrated compiler toolchain.
- Integrated QEMU ISA simulator with support for other industry standard instruction & cycle accurate simulators.
- High-level RISC-V register viewer.
- Integrated RTOS (e.g. FreeRTOS or Zephyr) debug support.
- Project wizards, templates & examples.

For more information on Ashling's *RiscFree* see: <u>https://www.ashling.com/ashling-riscv/</u> and for details on Renesas's RISC-V MCUs visit here: <u>https://www.renesas.com/us/en/about/press-room/renesas-unveils-first-generation-own-32-bit-risc-v-cpu-core-ahead-competition</u>

About Ashling

Ashling has been a leading provider of Embedded Development Tools & Services since 1982, with design centers in Limerick Ireland and Kochi India and sales and support offices in Europe, Asia Pacific, the Middle East, and America. The company has a particular focus on RISC-V and is the first to bring tools to the market supporting the heterogeneous debugging of RISC-V cores along with other cores from multiple vendors. Visit <u>https://www.ashling.com/</u> for more details.

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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